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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,968	07/25/2003	Lawrence T. Clark	ITL.0961US (P16065)	3944

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EXAMINER	
BRADLEY, MATTHEW A	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,968	CLARK ET AL.	
	Examiner	Art Unit	
	Matthew Bradley	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/6/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 6 October 2003 was filed after the mailing date of 25 July 2003 for application 10/626,968. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner is considering the information disclosure statement with a signed and initialed copy being attached hereto.

Specification

The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in **upper case, without underlining** or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC (See 37 CFR 1.52(e)(5) and MPEP 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text are permitted to be submitted on compact discs.) or
REFERENCE TO A "MICROFICHE APPENDIX" (See MPEP § 608.05(a). "Microfiche Appendices" were accepted by the Office until March 1, 2001.)
(f) BACKGROUND OF THE INVENTION.
(1) Field of the Invention.

(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(g) BRIEF SUMMARY OF THE INVENTION.

(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).

(i) DETAILED DESCRIPTION OF THE INVENTION.

(j) CLAIM OR CLAIMS (commencing on a separate sheet).

(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).

(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 11, 16, and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner notes that the entire "input virtual address" is claimed yet the data in the second memory portion is read before the "input virtual address entirely matches the input virtual address." Based on the input virtual address being available in its entirety before operations are preformed, the Examiner is interpreting that a portion of the input virtual address is being read and speculation is invoked to determine the rest of the address.

Any claims not specifically addressed are rejected to by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-11, and 21-25 are rejected under 35 U.S.C. 102(a) and (e) as being anticipated by Topham et al (U.S. 2002/0144078).

As per independent claim 1, Topham et al (herein after referred to as Topham) teach, reading a second memory portion that stores a specific physical address corresponding to an input virtual address before internally stored data accessed from a first memory portion based on the input virtual address entirely matches the input virtual address. (Paragraph 66 –67). *The Examiner notes that Topham maintains a partial lookup table that is used to speculate against virtual addresses. The partial physical*

address is formed from a partial frame number within the partial lookup table and the offset bits of a virtual address. This allows Topham to access the data being requested at the address before an entire match is recorded.

As per dependent claim 2, Topham teacheses, including using at least two register files, one for said first memory portion and the other for said second memory portion (Paragraph 72).

As per dependent claim 3, Topham teacheses, including decoding the input virtual address before accessing said at least two register files, wherein said at least two register files having a multiplicity of write and read ports that enable and simultaneously accessing to the internally stored data and said specific physical address output (Paragraph 71). *The Examiner notes that certain bits within the entire virtual address bit length are decoded to begin the selection of the partial frame number from the partial look up table.*

As per dependent claim 4, Topham teacheses, storing a multiplicity of tags in the internally stored data; receiving indexing data within the input virtual address; examining said indexing data to identify corresponding at least two tags from the internally stored data; comparing said indexing data with said at least two tags; and after any one of the tags of said at least two tags in the internally stored data matches said indexing data, signaling an enable signal to output the specific physical address output (Paragraph 84). *The Examiner notes that Topham maintains addresses with certain bit values that correspond to various components of the virtual to physical address translation process.*

As per dependent claim 5, Topham teacheses, storing an identifying data value in said one of said at least two register files for the specific physical address output; and storing a specific data associated with the identifying data value for the specific physical address output in the other register file of said at least two register files (Paragraph 73).

As per dependent claim 6, Topham teaches, accessing the second memory portion for the specific data before a match occurs between the identifying data value and the specific data (Paragraph 55).

As per independent claim 7, Topham teaches, reading a physical address value corresponding to a virtual address that includes an input data word for address translation of said virtual address into a specific data address; and comparing the input data word to internally stored data in parallel with said reading (Paragraph 66 and 69). *The Examiner notes that parallel comparing as claimed instantly is taught by Topham in paragraph 68 ("The full lookup table is accessed in parallel...").*

As per dependent claim 8, Topham teaches,

- selecting a page size for the virtual address; varying the number and position of compared bits for the virtual address based on the selected page size (Paragraph 53);
- and if any one of the internally stored data matches the input data word, signaling an enable signal to output the specific data address (Paragraph 72).

As per dependent claim 9, Topham teaches, defining a set associativity for a multiplicity of virtual memory locations that hold the internally stored data and translating

the virtual address using any one of the multiplicity of virtual memory locations based on the set associativity (Paragraph 53).

As per dependent claim 10, Topham teaches, storing the internally stored data in a first register file adapted to fire simultaneously with a second register file and decoding selected bits of the virtual address before accessing said first and second register files wherein the selected bits are indicative of a bank page size (Paragraph 72).

As per independent claim 11, Topham teaches, a data bank including a first memory portion to store internally stored data selectively accessible based on an input virtual address and a second memory portion accessible in parallel to said first memory portion to translate the input virtual address into a specific physical address before the internally stored data entirely matches the input virtual address (Paragraph 66 –67). *The Examiner notes that Topham maintains a partial lookup table that is used to speculate against virtual addresses. The partial physical address is formed from a partial frame number within the partial lookup table and the offset bits of a virtual address. This allows Topham to access the data being requested at the address before an entire match is recorded.*

As per independent claim 21, Topham teaches,

- a content addressed buffer (Paragraph 52)
- with a data bank including a first memory portion storing internally stored data selectively accessible based on an input virtual address and a second memory portion accessible in parallel to said first memory portion

for translation of the input virtual address into a specific physical address before the internally stored data entirely matches the input virtual address (Paragraph 72). *The Examiner notes that as discussed supra with respect to independent claim 7, the parallel accessing is taught by Topham et al in paragraph 68.*

As per dependent claim 22, Topham teaches, wherein said content addressed buffer is a set associative translation look aside buffer (Paragraph 52).

As per dependent claim 23, Topham teaches, said first memory portion is a virtual address register file, and said second memory portion is a physical address register file, wherein each of said virtual and physical address register files having a multiplicity of write and read ports (Paragraph 72).

As per dependent claim 24, Topham teaches, said first memory portion is a first static random access memory that stores a virtual address, and said second memory portion is a second static random access memory that stores a physical address (Paragraph 72).

As per dependent claim 25, Topham teaches, said content addressed buffer further includes a selector to select a page size for the input virtual address and a register to select the number and position of compared bits for the input virtual address based on the selected page size (Paragraph 52).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 12-15 are rejected under 35 U.S.C. 103(a) as being obvious over Topham et al. (U.S. 2002/0144078) in view of Riordan (U.S. 5,953,748).

As per dependent claim 12, Topham does teach the limitations of the independent claim 11 from with the dependent claim 12 relies upon.

Topham does not teach, including a multiplexer to select the specific physical address output from said data bank.

Riordan teaches, including a multiplexer to select the specific physical address output from said data bank (Column 5 lines 17-22).

Topham and Riordan are analogous art because they are from the same field of endeavor of speculative memory translation.

At the time of the invention, having the teachings of both Topham and Riordan before him or her, it would have been obvious to a person of ordinary skill in the art to include the multiplexers of Riordan into the system of Topham for the purpose of physical address selection.

The motivation for doing so would have been to allow the system of Topham to select the physical address "As soon as bits 12 to 15 of the virtual memory address are computed. (see Riordan Column 5 lines 15-17)" This decreases the amount of time required for the physical address selection due to the lesser number of bits being required before utilizing the multiplexers to determine the address.

Therefore it would have been obvious to combine Riordan with Topham for the benefit of physical address selection to obtain the invention as specified in claims 12-15.

As per dependent claim 13, Topham teaches, said first memory portion is a virtual address register file, and said second memory portion is a physical address register file, wherein each of said virtual and physical address register files having a multiplicity of write and read ports (Paragraph 72).

As per dependent claim 14, Topham teaches, further including a selector to select the number and position of compared bits for the input virtual address based on the page size selected (Paragraph 52), wherein said virtual address register file to store a multiplicity of tags in the internally stored data and said physical address register file to store the specific physical address output (Paragraph 72).

As per dependent claim 15, Topham teaches,

- an address selector to receive indexing data within the input virtual address to examine said indexing data and to identify corresponding at least two tags from the internally stored data; (Paragraph 66 –67)
- a decoder, coupled to said address selector, to decode the input virtual address before accessing said virtual and physical address register files to

enable simultaneous access to the internally stored data and said specific physical address output, respectively; (Paragraph 66 and 69)

- and a comparator, coupled to said decoder, to compare said indexing data with said at least two tags and after any one of the tags of said at least two tags in the internally stored data matches said indexing data, (Paragraph 72)

Riordan teaches:

- signaling an enable signal to said multiplexer to output the specific physical address output (Column 5 lines 17-22).

Claims 16-20 are rejected under 35 U.S.C. 103(a) as obvious over Topham et al (U.S. 2002/0144078) in view of Microsoft Computer Dictionary, Third Edition.

As per independent claim 16, Topham teaches,

- a processor having a (Figure 1 item 1, see Paragraph 46)
- content addressed buffer (Paragraph 52)
- with a data bank including a first memory portion storing internally stored data accessible selectively based on an input virtual address and a second memory portion accessible in parallel to said first memory portion for translation of the input virtual address into a specific physical address before the internally stored data entirely matches the input virtual address and the internally stored data; (Paragraph 66 –67). *The Examiner notes that Topham maintains a partial lookup table that is used to speculate against virtual addresses. The partial physical address is formed from a*

partial frame number within the partial lookup table and the offset bits of a virtual address. This allows Topham to access the data being requested at the address before an entire match is recorded.

Topham does not teach,

- and a flash memory coupled to said processor. (Paragraph 50).

The Microsoft Computer Dictionary Third Edition teaches that a flash memory "is commonly used as a supplement to or replacement for hard disks in portable computers."

At the time of invention, it would have been obvious to a person of ordinary skill in the art, having both the teachings of Topham and the Microsoft Computer Dictionary Third Edition before him/her, to supplement or replace the use of a hard disk drive in the system of Topham with a flash memory for the purpose of mobility.

The motivation for doing so is that a system of Topham with a flash memory promotes mobility allowing for the system to not only be employed upon stationary computing devices, but also on mobile devices.

Therefore it would have been obvious to combine Topham with a flash memory for the benefit of mobility to obtain the invention specified in claims 16-20.

As per dependent claim 17, Topham teaches, wherein said content addressed buffer is a set associative translation look aside buffer (Paragraph 52).

As per dependent claim 18, Topham teaches, said first memory portion is a virtual address register file, and said second memory portion is a physical address

register file, wherein each of said virtual and physical address register files having a multiplicity of write and read ports (Paragraph 72).

As per dependent claim 19, Topham teaches, said first memory portion is a first static random access memory that stores a virtual address, and said second memory portion is a second static random access memory that stores a physical address (Paragraph 72).

As per dependent claim 20, Topham teaches, said content addressed buffer further includes a selector to select a page size for the input virtual address and a register to select the number and position of compared bits for the input virtual address based on the selected page size (Paragraph 52).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. U.S. Patent Application Number 2004/0034756 Clark et al teach a parallel accessing method between virtual and physical.

2. U.S. Patent Application Number 2004/0019762 Fukuoka et al teach a virtual to physical address method.

3. U.S. Patent Application Number 2003/0046510 North teaches a virtual to physical address method.

4. U.S. Patent Application Number 2003/0018875 Henry et al teach a speculative forwarding apparatus and method.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew Bradley whose telephone number is (571) 272-8575. The examiner can normally be reached on 6:30-3:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald A. Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CPC/mb MB

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PRIMARY EXAMINER